CLAIMS

What is claimed is:

1. A multiplexer structure comprising:

a semiconductor substrate having a shared diffusion region;

a first gate disposed on the shared diffusion region, the first gate having a first finger and a second finger;

a second gate disposed on the shared diffusion region, the second gate having a first finger and a second finger;

a contact for a first input node disposed on the shared diffusion region between the first and second fingers of the first gate;

a contact for a second input node disposed on the shared diffusion region between the first and second fingers of the second gate;

a contact for a collector node disposed on the shared diffusion region between the first and second gates, wherein

closing the first gate electrically connects the first input node and the collector node, and

closing the second gate electrically connects the second input node and the collector node.

2. A multiplexer structure according to claim 1, wherein

the first gate, the first input node and the collector node define a first transistor element, and

the second gate, second input node and the collector node define a second transistor element.

3. A multiplexer structure according to claim 1, further comprising:

a first memory element connected to the first gate for closing the first gate; and

a second memory element connected to the second gate for closing the second gate.

4. A multiplexer structure according to claim 3, wherein a spacing between the first gate and the second gate is comparable to a linear dimension of the first memory element.

5. A multiplexer structure according to claim 1, further comprising:

a first input element connected to the first input node for providing input values to the first input node; and

a second input element connected to the second input node for providing input values to the second input node.

6. A programmable logic device, comprising: a multiplexer structure according to claim 1.

7. A data processing system, comprising: a programmable logic device according to claim 6.

8. A multiplexer structure comprising:

a semiconductor substrate having a plurality of shared diffusion regions;

a plurality of gates disposed on the substrate across the shared diffusion regions, each gate having a first finger and a second finger;

a plurality of contacts for input nodes disposed on the shared diffusion regions between the first and second fingers of the gates;

a plurality of contacts for collector nodes disposed on the shared diffusion regions between the gates, wherein closing a first gate electrically connects a corresponding input node enclosed by the first gate with adjacent collector nodes in the shared diffusion regions.

9. A multiplexer structure according to claim 8, wherein in each shared diffusion region a configuration of the first gate, an input node between the fingers of the first gate, and at least one collector node adjacent to the first gate defines a transistor element.

10. A multiplexer structure according to claim 8, further comprising: a plurality of memory elements connected to the gates for closing the gates.

11. A multiplexer structure according to claim 10, wherein a spacing between the gates is comparable to a linear dimension of the memory elements.

12. A multiplexer structure according to claim 8, further comprising: a plurality of input elements connected to the inputs nodes for providing input values to the input nodes.

13. A multiplexer structure according to claim 8, further comprising: a connecting element for electrically connecting the contacts of collector nodes across a first shared diffusion region so that the connecting element provides a multiplexer output from the input nodes in the first shared diffusion region.

14. A multiplexer structure according to claim 8, further comprising: a plurality of connecting elements for electrically connecting the contacts of collector nodes across the shared diffusion regions so that the connecting elements provide a multiplexer output stage from the input nodes in the shared diffusion regions.

15. A programmable logic device, comprising: a multiplexer structure according to claim 8.

16. A data processing system, comprising: a programmable logic device according to claim 15.

17. A method of providing a multiplexing structure, comprising:

providing a semiconductor substrate having a shared diffusion region;

disposing a first gate on the shared diffusion region, the first gate having a first finger and a second finger;

disposing a second gate on the shared diffusion region, the second gate having a first finger and a second finger;

disposing a contact for a first input node on the shared diffusion region between the first and second fingers of the first gate;

disposing a contact for a second input node on the shared diffusion region between the first and second fingers of the second gate;

disposing a contact for a collector node on the shared diffusion region between the first and second gates, wherein

closing the first gate electrically connects the first input node and the collector node, and

closing the second gate electrically connects the second input node and the collector node.

18. A method according to claim 17, wherein

the first gate, the first input node and the collector node define a first transistor element, and

the second gate, second input node and the collector node define a second transistor element.

19. A method according to claim 17, further comprising:

connecting a first memory element to the first gate for closing the first gate; and

connecting a second memory element to the second gate for closing the second gate.

20. A method according to claim 19, wherein a spacing between the first gate and the second gate is comparable to a linear dimension of the first memory element.

21. A method according to claim 17, further comprising:

connecting a first input element to the first input node for providing input values to the first input node; and

connecting a second input element connected to the second input node for providing input values to the second input node.

22. A method of providing a multiplexer structure comprising:

providing a semiconductor substrate having a plurality of shared diffusion regions;

disposing a plurality of gates on the substrate across the shared diffusion regions, each gate having a first finger and a second finger;

disposing a plurality of contacts for input nodes on the shared diffusion regions between the first and second fingers of the gates;

disposing a plurality of contacts for collector nodes on the shared diffusion regions between the gates, wherein closing a first gate electrically connects a corresponding input node enclosed by the first gate with adjacent collector nodes in the shared diffusion regions.

23. A method according to claim 22, wherein in each shared diffusion region a configuration of the first gate, an input node between the fingers of the first gate, and at least one collector node adjacent to the first gate defines a transistor element.

24. A method according to claim 22, further comprising: connecting a plurality of memory elements to the gates for closing the gates.

25. A method according to claim 24, wherein a spacing between the gates is comparable to a linear dimension of the memory elements.

26. A method according to claim 22, further comprising: connecting a plurality of input elements to the inputs nodes for providing input values to the input nodes.

27. A method according to claim 22, further comprising: providing a connecting element for electrically connecting the contacts of collector nodes across a first shared

diffusion region so that the connecting element provides a multiplexer output from the input nodes in the first shared diffusion region.

28. A method according to claim 22, further comprising: providing a plurality of connecting elements for electrically connecting the contacts of collector nodes across the shared diffusion regions so that the connecting elements provide a multiplexer output stage from the input nodes in the shared diffusion regions.